L Number	Hits	Search Text	DB	Time stamp
1	14952	((BOND OR BONDING) ADJ PAD)	USPAT; US-PGPUB	2004/11/12 11:28
2	9515	(((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)	USPAT; US-PGPUB	2004/11/12 10:45
3	7781	((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821	USPAT; US-PGPUB	2004/11/12 10:47
4	7523	(((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821) and (metal or conductor or conductive or conducting)	USPAT; US-PGPUB	2004/11/12 10:47
5	5929	(((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))	USPAT; US-PGPUB	2004/11/12 11:28
6	5929	((((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))) and device and @ad<20030821	USPAT; US-PGPUB	2004/11/12 10:47
7	2761	(((((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))) and device and @ad<20030821) and thick	USPAT; US-PGPUB	2004/11/12 10:48
8	454	((((((((BOND OR BONDING) ADJ PAD)) and (dielectric or insulating or insulator or insulative)) and device and @ad<20030821) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))) and device and @ad<20030821) and thick) and (crack or cracking)	USPAT; US-PGPUB	2004/11/12 10:48
9	12173	((BOND OR BONDING) ADJ PAD)	EPO; JPO; DERWENT; IBM_TDB	2004/11/12 11:28
10	1235	(((BOND OR BONDING) ADJ PAD)) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))	EPO; JPO; DERWENT; IBM_TDB	2004/11/12 11:29
11	54	((((BOND OR BONDING) ADJ PAD)) and ((metal or conductor or conductive or conducting) same (dielectric or insulating or insulator or insulative))) and thick	EPO; JPO; DERWENT; IBM_TDB	2004/11/12 11:29

L Number	Hits	Search Text	DB	Time stamp
1	753	(high adj current) and ((bond or bonding) adj pad)	USPAT; US-PGPUB	2004/11/12 14:03
2	707	((high adj current) and ((bond or bonding) adj pad)) and @ad<20030821	USPAT; US-PGPUB	2004/11/12 13:51
3	15	(high adj current) and ((bond or bonding) adj pad)	EPO; JPO; DERWENT; IBM_TDB	2004/11/12 14:03

US-PAT-NO: 6133054

DOCUMENT-IDENTIFIER: US 6133054 A

TITLE: Method and apparatus for testing an integrated circuit

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Brief Summary Text - BSTX (6):

In a typical wafer level burn-in application, multiple devices are connected in parallel to a common power supply or signal generator. The multiple devices connected to any single power supply or signal generator define a cluster or group. If one or more of the devices in a cluster is defective such that it draws an excessively large current when the burn-in test conditions are applied, the excessive current draw will prevent the power supply from providing the necessary voltages to the remaining devices in the cluster. When this situation occurs, the remaining devices in the cluster are prevented from being properly burned in. Without receiving proper burn-in, the remaining devices in the cluster typically must be discarded even if they are otherwise functional because the reliability of these devices has not been adequately determined. Thus, in a conventional wafer level burn-in application, fully functional and operational devices often must be discarded because conventional wafer level burn-in testing systems are incapable of isolating defective and **high current** devices from the remaining devices in the cluster such that the remaining devices receive a proper burn-in signal. While this problem could be addressed by dedicating separate drivers and power supplies to each device on

the wafer, the cost of doing so would be astronomical. The fear of discarding large numbers of functional devices because of a single bad device in a cluster motivates manufacturers to burn-in devices using small clusters, but small clusters result in extra testing cost in the form of additional probing hardware required to probe each cluster and additional power supplies and logic signal generators for each cluster. Therefore, it is highly desirable to provide a solution enabling the wafer level burn-in testing of multiple integrated circuits that is capable of isolating non-functional or defective devices from the burn-in signals during the burn-in test such that the remaining devices receive an adequate burn-in test. It is further desirable that the implemented solution does not significantly increase the hardware required to perform the wafer level burn-in and does not otherwise significantly increase the cost or time required to complete the burn-in.

Detailed Description Text - DETX (13):

use of space and its simplicity, the serpentine fuse structure 106 of FIG. 4 is desirable for its ability to blow at lower currents than fuse structure of 106 of FIG. 3. It is theorized that fuse structure 106 of FIG. 3 requires a higher current to create an open circuit because the fusible link 300 is surrounded by a field of passivation or other dielectric material that can effectively act as a heat sink to reduce the temperature of fusible link 300 and thereby resulting in a greater fuse current required to achieve the fuse temperature needed to melt or otherwise blow the fuse. In contrast, the serpentine circuit 106 of FIG. 4 radiates its thermal energy to remaining portions of fusible link 300. In this manner, the

serpentine structure of FIG. 4 provides a positive feedback mechanism in which a **high current** density increases the temperature within fusible link 300 and the higher temperature is radiated to other portions of the fusible link thereby further raising the temperature of fusible link 300 thereby resulting in the generation of a sufficient melting temperature at a significantly lower current value. FIG. 5 presents an extension of the serpentine structure of FIG. 4 in which two or more fuses 106 and fusible links 300 from corresponding conductive members 110 are intertwined such that the thermal energy radiated by one of the links 300 results in the destruction of neighboring fusible links 300. This embodiment is advantageous in an application, for example, where it is desirable to ensure that all signals are disconnected from a circuit whenever any of the remaining signals is disconnected. If, for example, the VDD power supply signal in an integrated circuit device 104 draws a significant current that results in the destruction of its associated fuse structure 106, the remaining clock signals and data signals for that device will continue to be exercised. This may result in a condition in which the ESD circuitry connected to each of these input pads becomes forward biased. When this situation occurs, the clock or data signal associated with the forward biased ESD diode will be unable to drive the appropriate voltage on the corresponding conductive member 110 thereby affecting the burn-in of the remaining good devices. To prevent such an occurrence, it is desirable in one embodiment to blow all fuses 106 associated with a particular integrated circuit device 104 if any of the fuses associated with that device are blown. To accomplish this goal, the intertwined serpentine structure of FIG. 5 contemplates a

layout designed to
insure that the physical destruction of one fuse structures
300 will cause the
physical destruction of neighboring fusible links 300.